Cross-Reference to Related Applications

This continuation application claims priority from currently pending U.S. Patent Application Serial No. 10/202,556, entitled "Method and Apparatus for Regulating Predriver for Output Buffer," filed July 23, 2002, now U.S. Patent No. 6,707,722 and hereby incorporated herein by reference.

TNT 08/20/04

In the Specification

Please replace paragraph [0014] as follows:

Figure 2 illustrates [a] an I-V diagram for operation for a pull-down transistor device configured with a prior art predriver circuit;

Please replace paragraph [0015] as follows:

Figure 3 illustrates an exemplary embodiment of an electronic system with a memory system in accordance with the present invention;

Please replace paragraph [0018] as follows:

Figure 10 illustrates an I-V diagram for operation for a pull-down element configured with a regulated predriver for an output buffer in accordance with an exemplary embodiment of the present invention.

Please replace paragraph [0040] as follows:

In addition, with reference to an output buffer 700 illustrated in Figure 7, a limiter circuit 706 can also be configured in [an] a p-channel diode clamp arrangement. Limiter circuit 706 comprises one or more p-channel devices connected in a diode manner, e.g., p-channel transistors M_{P1}, M_{P2}, and M_{P3}. Again, gate voltage V_{GATE} is limited by the number of P-channel devices times the threshold voltage V_{TP}, e.g., for 3 x V_{TP}, with a threshold voltage V_{TP} =0.9 volts, V_{GATE} is limited to 2.7 volts. Still further, instead of using diode-connected p-channel or n-channel transistors, with reference to an output buffer 800 illustrated in Figure 8, a limiter circuit 806 can also be